CMOS Switched-Capacitor Voltage Converter

ADM660/ADM8660

FEATURES
ADM660: Inverts or Doubles Input Supply Voltage
ADM8660: Inverts Input Supply Voltage
100 mA Output Current
Shutdown Function (ADM8660)
2.2 μF or 10 μF Capacitors
0.3 V Drop at 30 mA Load
+1.5 V to +7 V Supply
Low Power CMOS: 600 μA Quiescent Current
Selectable Charge Pump Frequency (25 kHz/120 kHz)
Pin Compatible Upgrade for MAX660, MAX665, ICL7660

APPLICATIONS
Handheld Instruments
Portable Computers
Remote Data Acquisition
Op Amp Power Supplies

GENERAL DESCRIPTION

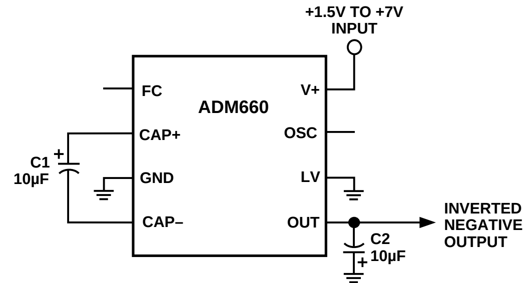
The ADM660/ADM8660 is a charge-pump voltage converter that can be used to either invert the input supply voltage giving $V_{OUT} = –V_{IN}$ or double it (ADM660 only) giving $V_{OUT} = 2 \times V_{IN}$.

Input voltages ranging from +1.5 V to +7 V can be inverted into a negative –1.5 V to –7 V output supply. This inverting scheme is ideal for generating a negative rail in single power-supply systems. Only two small external capacitors are needed for the charge pump. Output currents up to 50 mA with greater than 90% efficiency are achievable, while 100 mA achieves greater than 80% efficiency.

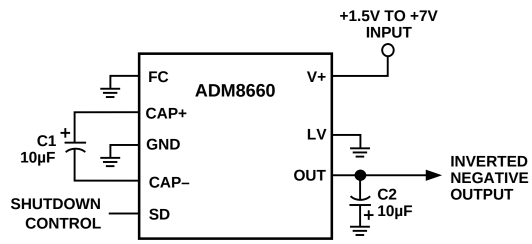
A Frequency Control (FC) input pin is used to select either 25 kHz or 120 kHz charge-pump operation. This is used to optimize capacitor size and quiescent current. With 25 kHz selected, a 10 μF external capacitor is suitable, while with 120 kHz, the capacitor may be reduced to 2.2 μF. The oscillator frequency on the ADM660 can also be controlled with an external capacitor connected to the OSC input or by driving this input with an external clock. In applications where a higher supply voltage is desired it is possible to use the ADM660 to double the input voltage. With input voltages from 2.5 V to 7 V, output voltages from 5 V to 14 V are achievable with up to 100 mA output current.

The ADM8660 features a low power shutdown (SD) pin instead of the external oscillator (OSC) pin. This can be used to disable the device and reduce the quiescent current to 300 nA.

TYPICAL CIRCUIT CONFIGURATIONS



Voltage Inverter Configuration (ADM660)



Voltage Inverter Configuration with Shutdown (ADM8660)

The ADM660 is a pin compatible upgrade for the MAX660, MAX665, ICL7660 and LTC1046.

The ADM660/ADM8660 is available in 8-pin DIP and narrow-body SOIC.

ADM660/ADM8660 Options

Option	ADM660	ADM8660
Inverting Mode	Y	Y
Doubling Mode	Y	N
External Oscillator	Y	N
Shutdown	N	Y
Package Options		
SO-8	Y	Y
N-8	Y	Y

REV. 0

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ADM660/ADM8660–SPECIFICATIONS (V+ = +5 V, C1, C2 = 10 μF,[1] $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted)

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Input Voltage, V+					R_L = 1 kΩ
	3.5		7.0	V	Inverting Mode, LV = Open
	1.5		7.0	V	Inverting Mode, LV = GND
	2.5		7.0	V	Doubling Mode, LV = OUT
Supply Current					No Load
		0.6	1	mA	FC = Open (ADM660), GND (ADM8660)
		2.5	4.5	mA	FC = V+, LV = Open
Output Current	100			mA	
Output Resistance		9	15	Ω	I_L = 100 mA
Charge-Pump Frequency		25		kHz	FC = Open (ADM660), GND (ADM8660)
		120		kHz	FC = V+
OSC Input Current		±5		μA	FC = Open (ADM660), GND (ADM8660)
		±25		μA	FC = V+
Power Efficiency (FC = Open)	90	94		%	R_L = 1 kΩ Connected from V+ to OUT
	90	93		%	R_L = 500 Ω Connected from OUT to GND
		81.5		%	I_L = 100 mA to GND
Voltage Conversion Efficiency	99	99.96		%	No Load
Shutdown Supply Current, I_{SHDN}		0.3	5	μA	ADM8660, SHDN = V+
Shutdown Input Voltage, V_{SHDN}	2.4			V	SHDN High = Disabled
			0.8	V	SHDN Low = Enabled
Shutdown Exit Time		500		μs	I_L = 100 mA

NOTES

[1]C1 and C2 are low ESR (<0.2 Ω) electrolytic capacitors. High ESR will degrade performance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

Input Voltage (V+ to GND, GND to OUT) . . . . +7.5 V
LV Input Voltage . . . . (OUT – 0.3 V) to (V+, + 0.3 V)
FC and OSC Input Voltage
. . . . (OUT – 0.3 V) or (V+, –6 V) to (V+, + 0.3 V)
OUT, V+ Output Current (Continuous) . . . . 120 mA
Output Short Circuit Duration to GND . . . . 10 secs
Power Dissipation, N-8 . . . . 625 mW
(Derate 8.3 mW/°C above +50°C)
θ_{JA}, Thermal Impedance . . . . 120°C/W
Power Dissipation R-8 . . . . 450 mW
(Derate 6 mW/°C above +50°C)
θ_{JA}, Thermal Impedance . . . . 170°C/W
Operating Temperature Range
Industrial (A Version) . . . . –40°C to +85°C
Storage Temperature Range . . . . –65°C to +150°C
Lead Temperature Range (Soldering 10 sec) . . . . +300°C
Vapor Phase (60 sec) . . . . +215°C
Infrared (15 sec) . . . . +220°C
ESD Rating . . . . >2000 V

NOTES

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model*	Temperature Range	Package Option
ADM660AN	–40°C to +85°C	N-8
ADM660AR	–40°C to +85°C	SO-8
ADM8660AN	–40°C to +85°C	N-8
ADM8660AR	–40°C to +85°C	SO-8

*N = Plastic DIP; R = SOIC.

PIN FUNCTION DESCRIPTIONS

Inverter Configuration

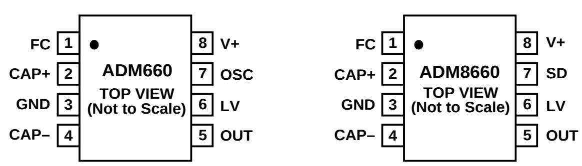
Mnemonic	Function
FC	Frequency Control Input for Internal Oscillator and Charge Pump. With FC = Open (ADM660) or connected to GND (ADM8660), f_{CP} = 25 kHz; with FC = V+, f_{CP} = 120 kHz
CAP+	Positive Charge-Pump Capacitor Terminal.
GND	Power Supply Ground.
CAP–	Negative Charge-Pump Capacitor Terminal.
OUT	Output, Negative Voltage.
LV	Low Voltage Operation Input. Connect to GND when input voltage is less than 3.5 V. Above 3.5 V, LV may be connected to GND or left unconnected.
OSC	ADM660: Oscillator Control Input. OSC is connected to an internal 15 pF capacitor. An external capacitor may be connected to slow the oscillator. An external oscillator may also be used to overdrive OSC. The charge-pump frequency is equal to 1/2 the oscillator frequency.
SD	ADM8660: Shutdown Control Input. This input, when high, is used to disable the charge pump thereby reducing the power consumption.
V+	Positive Power Supply Input.

Doubler Configuration (ADM660 Only) Configuration

Mnemonic	Function
FC	Frequency Control Input for Internal Oscillator and Charge Pump. With FC = Open, f_{CP} = 25 kHz; with FC = V+, f_{CP} = 120 kHz.
CAP+	Positive Charge-Pump Capacitor Terminal.
GND	Positive Input Supply.
CAP–	Negative Charge-Pump Capacitor Terminal.
OUT	Ground.
LV	Low Voltage Operation Input. Connect to OUT.
OSC	Must be left unconnected in this mode.
V+	Doubled Positive Output.

PIN CONNECTIONS

8-Pin



ADM660/ADM8660–Typical Performance Characteristics

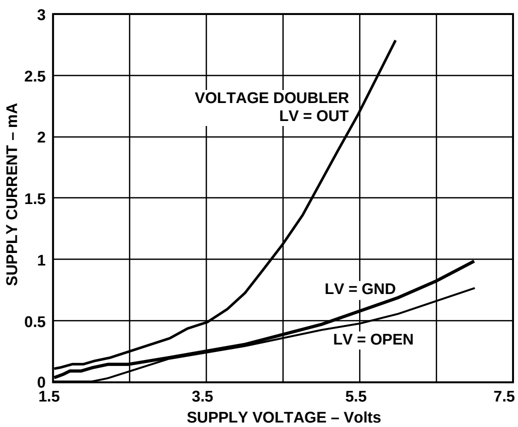


Figure 1. Power Supply Current vs. Voltage

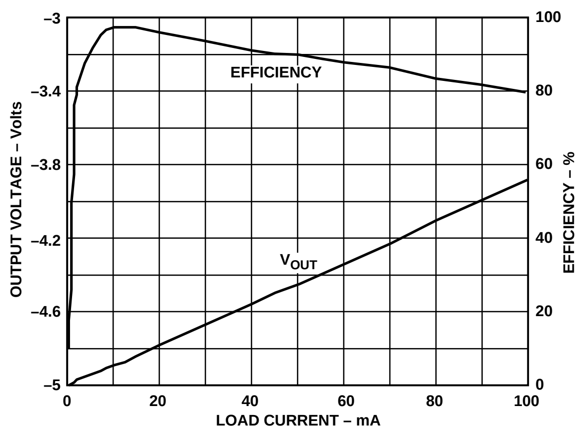


Figure 2. Output Voltage and Efficiency vs. Load Current

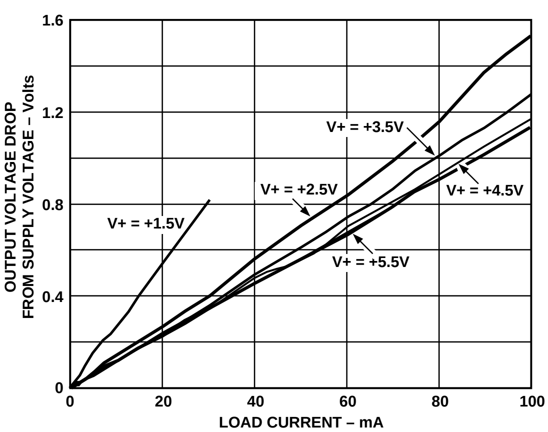


Figure 3. Output Voltage Drop vs. Load Current

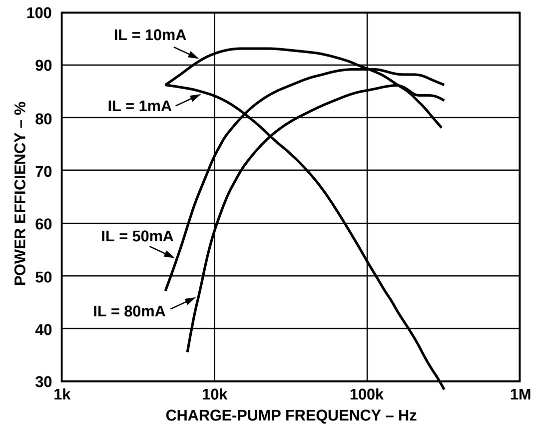


Figure 4. Efficiency vs. Charge-Pump Frequency

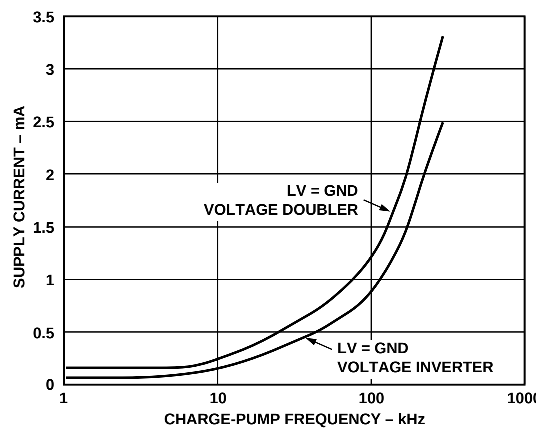


Figure 5. Power Supply Current vs. Charge-Pump Frequency

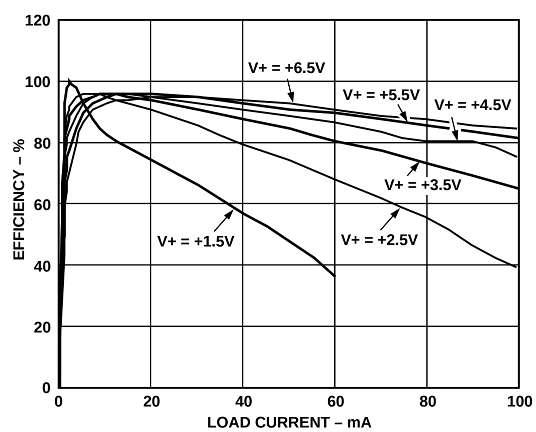


Figure 6. Power Efficiency vs. Load Current

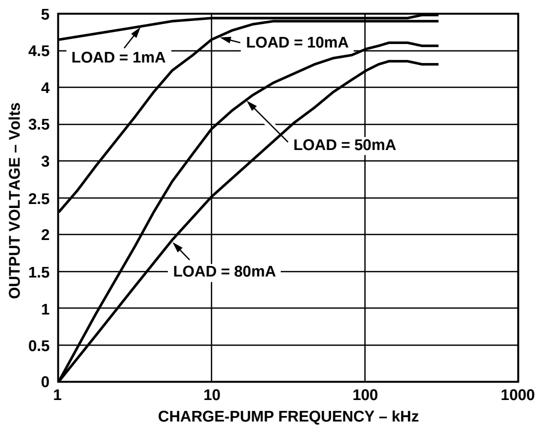


Figure 7. Output Voltage vs. Charge-Pump Frequency

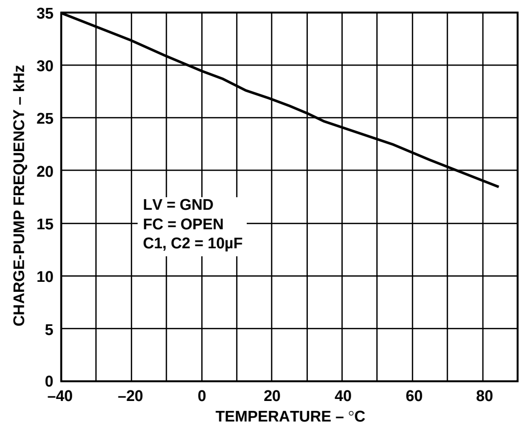


Figure 10. Charge-Pump Frequency vs. Temperature

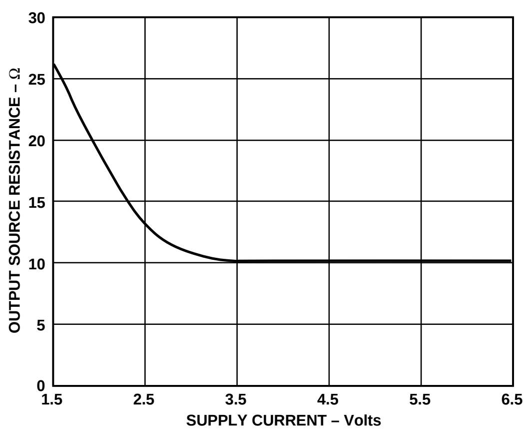


Figure 8. Output Source Resistance vs. Supply Voltage

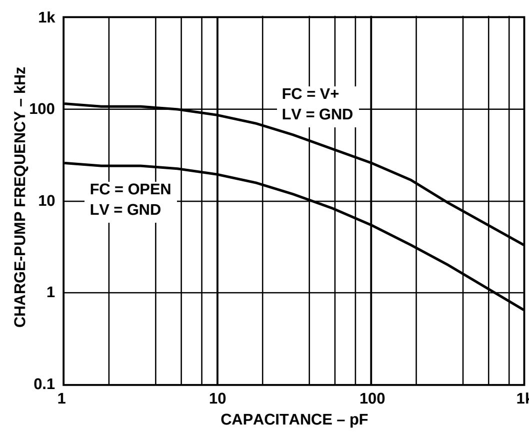


Figure 11. Charge-Pump Frequency vs. External Capacitance

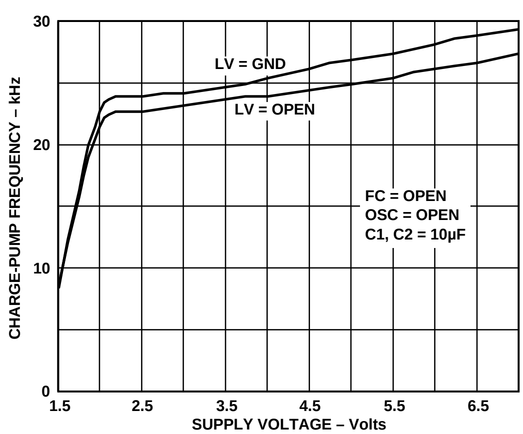


Figure 9. Charge-Pump Frequency vs. Supply Voltage

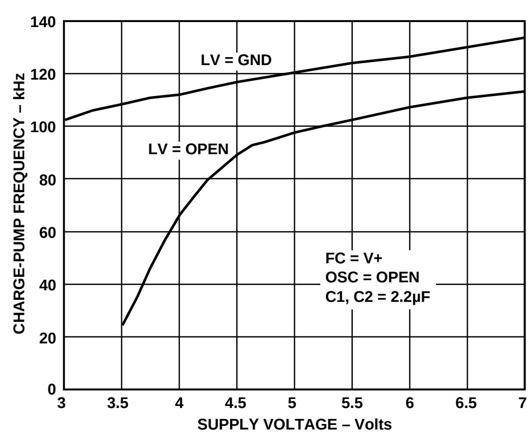


Figure 12. Charge-Pump Frequency vs. Supply Voltage

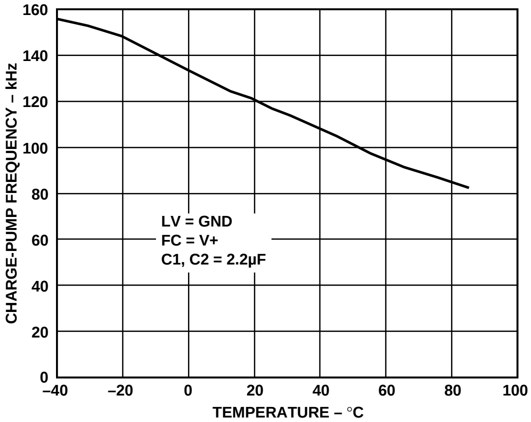


Figure 13. Charge-Pump Frequency vs. Temperature

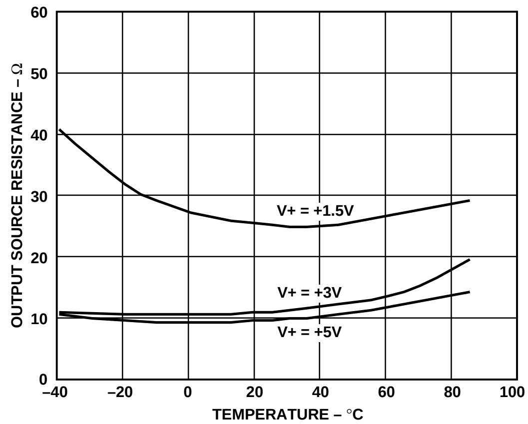


Figure 14. Output Resistance vs. Temperature

GENERAL INFORMATION

The ADM660/ADM8660 is a switched capacitor voltage converter that can be used to invert the input supply voltage. The ADM660 can also be used in a voltage doubling mode. The voltage conversion task is achieved using a switched capacitor technique using two external charge storage capacitors. An on-board oscillator and switching network transfers charge between the charge storage capacitors. The basic principle behind the voltage conversion scheme is illustrated in Figures 15 and 16.

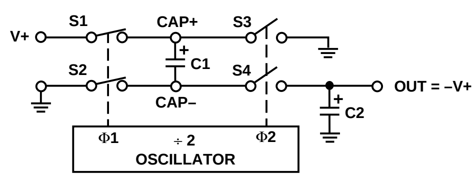


Figure 15. Voltage Inversion Principle

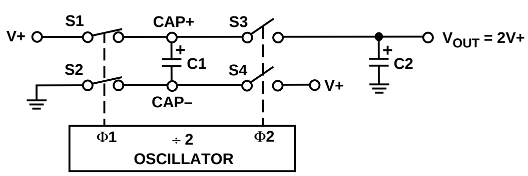


Figure 16. Voltage Doubling Principle

Figure 15 shows the voltage inverting configuration while Figure 16 shows the configuration for voltage doubling. An oscillator generating antiphase signals $\phi 1$ and $\phi 2$ controls switches S1, S2 and S3, S4. During $\phi 1$, switches S1 and S2 are closed charging C1 up to the voltage at V+. During $\phi 2$, S1 and S2 open and S3 and S4 close. With the voltage inverter configuration during $\phi 2$ the positive terminal of C1 is connected to GND via S3 and the negative terminal of C1 connects to V_{OUT} via S4. The net result is voltage inversion at V_{OUT} wrt GND. Charge on C1 is transferred to C2 during $\phi 2$. Capacitor C2 maintains this voltage during $\phi 1$. The charge transfer efficiency depends on the on-resistance of the switches, the frequency at which they are being switched and also on the equivalent series resistance (ESR) of the external capacitors. The reason for this is explained in the following section. For maximum efficiency, capacitors with low ESR are, therefore, recommended.

The voltage doubling configuration reverses some of the connections but the same principle applies.

Switched Capacitor Theory of Operation

As already described, the charge pump on the ADM660/ADM8660 uses a switched capacitor technique in order to invert or double the input supply voltage. Basic switched capacitor theory is discussed below.

A switched capacitor building block is illustrated in Figure 17. With the switch in position A, capacitor C1 will charge to voltage V1. The total charge stored on C1 is q1 = C1V1. The switch is then flipped to position B discharging C1 to voltage V2. The charge remaining on C1 is q2 = C1V2. The charge transferred to the output V2 is, therefore, the difference between q1 and q2, so $\Delta q = q1 - q2 = C1\,(V1 - V2)$.

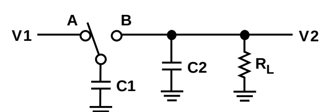


Figure 17. Switched Capacitor Building Block

As the switch is toggled between A and B at a frequency f, the charge transfer per unit time or current is

$$I = f(\Delta q) = f(C1)(V1 - V2)$$

Therefore

$$I = (V1 - V2)/(1/fC1) = (V1 - V2)/(R_{EQ})$$

where R_{EQ} = 1/fC1

The switched capacitor may, therefore, be replaced by an equivalent resistance whose value is dependent on both the capacitor size and on the switching frequency. This, therefore, explains why lower capacitor values may be used with higher switching frequencies. It should be remembered of course that as the switching frequency is increased the power consumption will increase due to some charge being lost at each switching cycle. At high frequencies, the power efficiency, therefore, starts decreasing. Other losses include the resistance of the internal switches and also the equivalent series resistance (ESR) of the charge storage capacitors.

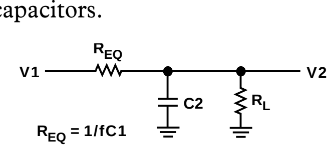


Figure 18. Switched Capacitor Equivalent Circuit

Inverting Negative Voltage Generator

Figures 19 and 20 show the ADM660/ADM8660 configured to generate a negative output voltage. Input supply voltages from 1.5 V up to 7 V are allowable. For supply voltage less than 3 V, LV must be connected to GND. This bypasses the internal regulator circuitry and gives best performance in low voltage applications. With supply voltages greater than 3 V, LV may be either connected to GND or left open. Leaving it open facilitates direct substitution for the ICL7660.

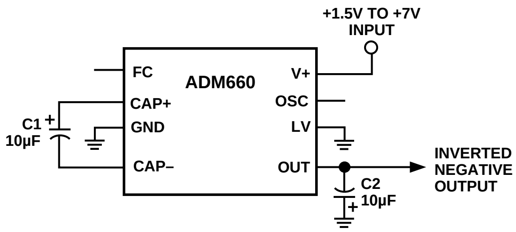


Figure 19. ADM660 Voltage Inverter Configuration

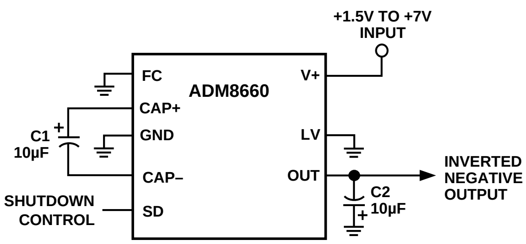


Figure 20. ADM8660 Voltage Inverter Configuration

OSCILLATOR FREQUENCY

The internal charge-pump frequency may be selected to be either 25 kHz or 120 kHz using the Frequency Control (FC) input. With FC unconnected (ADM660) or connected to GND (ADM8660), the internal charge pump runs at 25 kHz, while if FC is connected to V+, the frequency is increased by a factor of five. Increasing the frequency allows smaller capacitors to be used for equivalent performance or if the capacitor size is unchanged, it results in lower output impedance and ripple.

If an charge-pump frequency other than the two fixed values is desired, then this is made possible by the OSC input which can either have a capacitor connected to it or it may be overdriven by an external clock. Please refer to the Typical Performance Characteristics which shows the variation in charge-pump frequency versus capacitor size. The charge pump frequency is 1/2 the oscillator frequency applied to the OSC pin.

If an external clock is used to overdrive the oscillator its levels should swing to within 100 mV of V+ and GND. A CMOS driver is, therefore, suitable. When OSC is overdriven, FC has no effect but LV must be grounded.

Note that overdriving is only permitted in the voltage inverter configuration.

Table I. ADM660 Charge-Pump Frequency Selection

FC	OSC	Charge Pump	C1, C2
Open	Open	25 kHz	10 µF
V+	Open	120 kHz	2.2 µF
Open or V+	Ext Cap	See Typical Characteristics	
Open	Ext CLK	Ext CLK Frequency/2	

Table II. ADM8660 Charge-Pump Frequency Selection

FC	OSC	Charge Pump	C1, C2
GND	Open	25 kHz	10 µF
V+	Open	120 kHz	2.2 µF
GND or V+	Ext Cap	See Typical Characteristics	
GND	Ext CLK	Ext CLK Frequency/2	

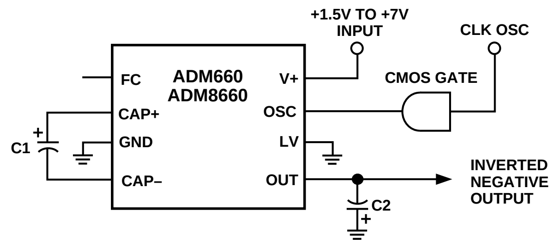


Figure 21. ADM660/ADM8660 External Oscillator

Voltage Doubling Configuration

Figure 22 shows the ADM660 configured to generate increased output voltages. As in the inverting mode, only two external capacitors are required. The doubling function is achieved by reversing some connections to the device. The input voltage is applied to the GND pin and V+ is used as the output. Input voltages from 2.5 V to 7 V are allowable. In this configuration, pins LV, OUT must be connected to GND.

The unloaded output voltage in this configuration is 2 (V_{IN}). Output resistance and ripple are similar to the voltage inverting configuration.

Note that the ADM8660 cannot be used in the voltage doubling configuration.

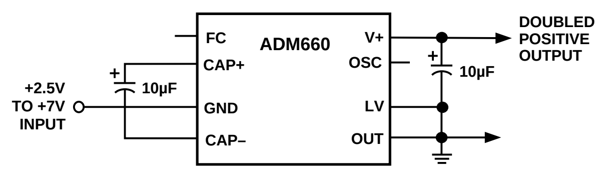


Figure 22. Voltage Doubler Configuration

Shutdown Input

The ADM8660 contains a shutdown input that can be used to disable the device and hence reduce the power consumption. A logic high level on the SD input shuts the device down reducing the quiescent current to 0.3 µA. During shutdown the output voltage goes to 0 V. Therefore, ground referenced loads are not powered during this state. When exiting shutdown it takes several cycles (approximately 500 µs) for the charge pump to reach its final value. If the shutdown function is not being used, then SD should be hardwired to GND.

Capacitor Selection

The optimum capacitor value selection depends the charge-pump frequency. With 25 kHz selected, 10 µF capacitors are recommended, while with 120 kHz selected, 2.2 µF capacitors may be used. Other frequencies allow other capacitor values to be used. For maximum efficiency in all cases, it is recommended that capacitors with low ESR are used for the charge pump. Low ESR capacitors give both the lowest output resistance and lowest ripple voltage. High output resistances degrades the overall power efficiency and causes voltage drops especially at high

output current levels. The ADM660/ADM8660 is tested using low ESR, 10 µF, capacitors for both C1 and C2. Smaller values of C1 increases the output resistance, while increasing C1 will reduce the output resistance. The output resistance is also dependent on the internal switches on-resistance as well as the capacitors ESR so the effect of increasing C1 becomes negligible past a certain point.

Figure 23 shows how the output resistance varies with oscillator frequency for three different capacitor values. At low oscillator frequencies, the output impedance is dominated by the $1/f_C$ term. This explains why the output impedance is higher for smaller capacitance values. At high oscillator frequencies, the $1/f_C$ term becomes insignificant and the output impedance is dominated by the internal switches on resistance. From an output impedance viewpoint, therefore, there is no benefit to be gained from using excessively large capacitors.

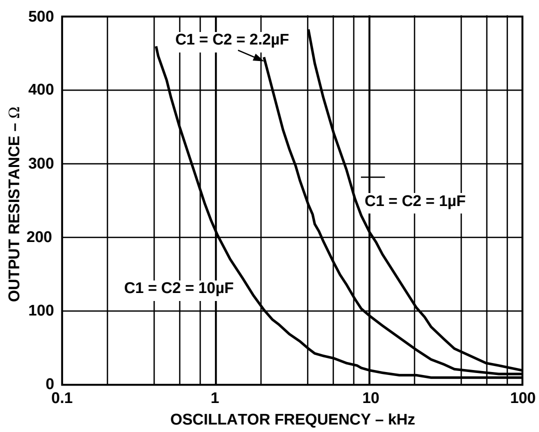


Figure 23. Output Impedance vs. Oscillator Frequency

Capacitor C2

The output capacitor size C2 affects the output ripple. Increasing the capacitor size reduces the peak-peak ripple. The ESR affects both the output impedance and the output ripple. Reducing the ESR reduces the output impedance and ripple. For convenience it is recommended that both C1 and C2 are the same value.

Table III. Capacitor Selection

Charge-Pump Frequency	Capacitor C1, C2
25 kHz	10 µF
120 kHz	2.2 µF

Power Efficiency and Oscillator Frequency Tradeoff

While higher switching frequencies allow smaller capacitors to be used for equivalent performance or indeed improved performance with the same capacitors, there is a tradeoff to be considered. As the oscillator frequency is increased, the quiescent current increases. This happens as a result of a finite charge being lost at each switching cycle. The charge loss per unit cycle at very high frequencies can be significant thereby reducing the power efficiency. Since the power efficiency is also degraded at low oscillator frequencies due to an increase in output impedance, this therefore means that there is an optimum frequency band for maximum power transfer. Please refer to the *"Typical Performance Characteristics"* section.

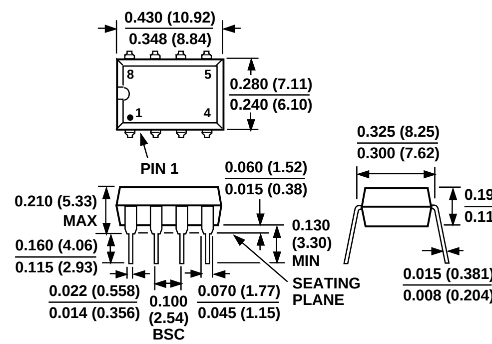
Bypass Capacitor

The ac impedance of the ADM660/ADM8660 may be reduced by using a bypass capacitor on the input supply. This capacitor should be connected between the input supply and GND. It will provide instantaneous current surges as required. Suitable capacitors of 0.1 µF or greater may be used.

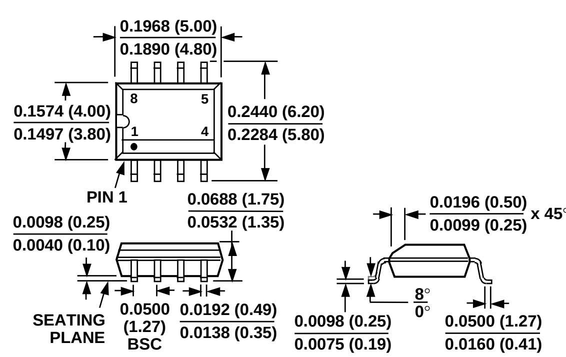
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead Plastic DIP (N-8)



8-Lead Narrow-Body SOIC (SO-8)



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